ABSTRACT OF DICLOSURE

An apparatus of a digital echo canceller comprises a first-set delay circuits, a selector, a second-set delay circuits, a plurality of multipliers and an adder. The first-set delay circuits are arranged into groups, and each group has N delay circuits. An exhaustive search function is carried out to produce a plurality of energy sums. The selector will select the biggest energy sum to serve as a significant part and then transmit to the outputs of the second-set delay circuits, the multipliers and the adder. An estimated echo signal is produced to cancel the echo signal.